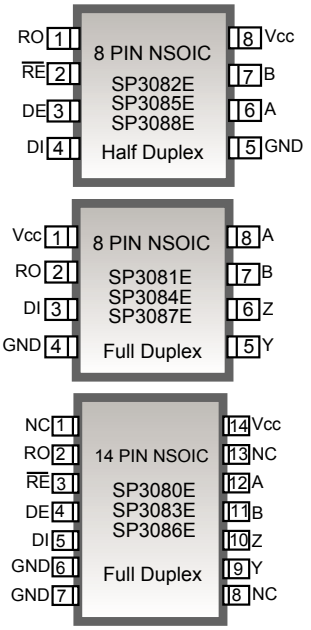
SP3080E-3088E

Advanced-Failsafe RS-485/RS-422 Transceivers
1/8th Unit Load, Slew-Rate Limited, ±15kV ESD-Protected

FEATURES

- 5.0V single supply operation
- Receiver failsafe on open, shorted or terminated lines
- 1/8th Unit Load, 256 transceivers on bus
- Robust ESD protection for RS-485 pins
  - o ±15kV Air-Gap Discharge
  - o ±15kV Human Body Model
  - o ±8kV Contact Discharge
- Controlled driver slew rates
  - o 115kbps, Low EMI (SP3080E, SP3081E, SP3082E)
  - o 500kbps, Low EMI (SP3083E, SP3084E, SP3085E)
  - o High Speed, 20Mbps (SP3086E, SP3087E, SP3088E)
- Hot Swap glitch protection on control inputs
- Driver short circuit current limit and thermal shutdown for overload protection
- Ultra-low 400µA quiescent current
- 1µA shutdown mode (except SP3081, SP3084, SP3087)
- Industry standard package footprints



APPLICATIONS

- Motor Control
- Building Automation
- Security Systems
- Remote Meter Reading
- Long or un-terminated transmission lines

DESCRIPTION

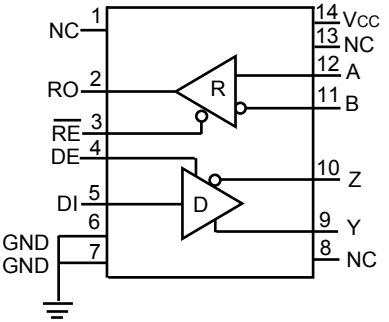
The SP3080E-SP3088E family of RS-485 devices are designed for reliable, bidirectional communication on multipoint bus transmission lines. Each device contains one differential driver and one differential receiver. SP3082E, SP3085E and SP3088E are half-duplex devices; other part numbers are full-duplex. All devices comply with TIA/EIA-485 and TIA/EIA-422 standards. Lead-free and RoHS compliant packages are available for all models.

These devices are ruggedized for use in harsh operating conditions over the entire common-mode voltage range from -7V to +12V. Receivers are specially designed to fail-safe to a logic high output state if the inputs are left un-driven or shorted. All RS-485 bus-pins are protected against severe ESD events up to ±15kV (Air-Gap and Human Body Model) and up to ±8kV Contact Discharge (IEC 1000-4-2). Drivers are protected from excess current flow caused by bus contention or output short-circuits by both an internal current limit and a thermal-overload shutdown. Devices are rated for industrial (-40 to +85ºC) operating temperatures. Receivers have exceptionally high input impedance, which places only 1/8th the standard load on a shared bus. Up to 256 transceivers may coexist while preserving full signal margin.

All devices operate from a single 5.0V power supply and draw negligible quiescent power. All versions except the SP3081E, SP3084E, and SP3087E may independently enable and disable their driver and receiver and enter a low power shutdown mode if both driver and receiver are disabled. All outputs maintain high impedance in shutdown or when powered-off.

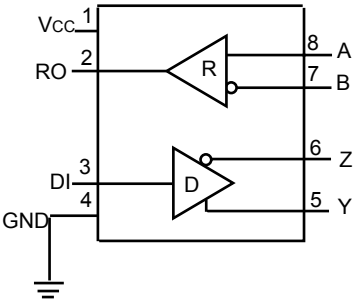
DEVICE ARCHITECTURE AND BLOCK DIAGRAMS

Devices are available in three industry standard architectures and footprints. In each footprint there are three speed grades available.



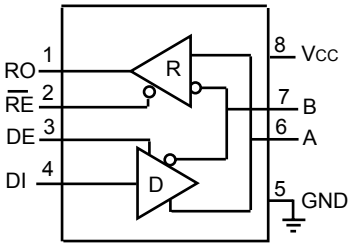
14-Pin Full Duplex

SP3080E, 115kbps slew rate limited
SP3083E, 500kbps slew rate limited
SP3086E, 20Mbps



8-Pin Full Duplex

SP3081E, 115kbps slew rate limited
SP3084E, 500kbps slew rate limited
SP3087E, 20Mbps



8-Pin Half Duplex

SP3082E, 115kbps slew rate limited
SP3085E, 500kbps slew rate limited
SP3088E, 20Mbps

Pin Number			Pin Name	Pin Function
Full-Duplex		Half - Duplex		
SP3080E	SP3081E	SP3082E		
SP3083E	SP3084E	SP3085E		
SP3086E	SP3087E	SP3088E		
2	2	1	RO	Receiver Output. When $\overline{RE}$ is low and if (A – B) ≥ -40mV, RO is high. If (A – B) ≤ - 200mV, RO is low.
3	-	2	$\overline{RE}$	Receiver Output Enable. When $\overline{RE}$ is low, RO is enabled. When $\overline{RE}$ is high, RO is high impedance. Drive $\overline{RE}$ high and DE low to enter shutdown mode. $\overline{RE}$ is a hot-swap input.
4	-	3	DE	Driver Output Enable. When DE is high, outputs are enabled. When DE is low, outputs are high impedance. Drive DE low and $\overline{RE}$ high to enter shutdown mode. DE is a hot-swap input.
5	3	4	DI	Driver Input. With DE high, a low level on DI forces non-inverting output low and inverting output high. A high level on DI forces non-inverting output high and inverting output low.
6, 7	4	5	GND	Ground
9	5	-	Y	Non-inverting Driver Output
10	6	-	Z	Inverting Driver Output
11	7	-	B	Inverting Receiver Input
-	-	7	B	Inverting Receiver Input and Inverting Driver Output
12	8	-	A	Non-inverting Receiver Input
-	-	6	A	Non-inverting Receiver Input and Non-inverting Driver Output
14	1	8	V_{CC}	Positive Supply V_{CC}. Bypass to GND with a 0.1uF capacitor.
1, 8, 13	-	-	NC	No Connect, not internally connected

Note: On 14-pin packages connect both pins 6 and 7 to Ground.

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Supply Voltage (V_{CC}).....+ 7.0V
Input voltage at control input pins ($\overline{RE}$, DE) ..... -0.3V to V_{CC}+0.3V
Driver input voltage (DI) .....-0.3V to V_{CC}+0.3V
Driver output voltage (A, B, Y, and Z) .....+/-13V
Receiver output voltage (RO) .....-0.3V to (Vcc + 0.3V)
Receiver input voltage (A, B) .....+/-13V
Package Power Dissipation:
Maximum Junction Temperature 150°C
8-Pin SO Θ_{JA} = 128.4°C/W
14-Pin SO Θ_{JA} = 86°C/W
Storage Temperature.....-65°C to +150°C
Lead Temperature (soldering, 10s)..... +300°C

RECOMMENDED OPERATING CONDITIONS

Vcc=5V ±5%, T_{MIN} to T_{MAX}, unless otherwise noted, Typical values are Vcc=5V and T_A=25°C

Recommended Operating Conditions		Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}		4.5	5	5.5	V
Input Voltage on A and B pins		-7		12	V
High-level input voltage (DI, DE or $\overline{RE}$), V_{IH}		2		V_{CC}	V
Low-level input voltage (DI, DE or $\overline{RE}$), V_{IH}		0		0.8	V
Output Current	Driver	-60		60	mA
	Receiver	-8		8	
Signaling Rate, 1/t_{UI}	SP3080, SP3081, SP3082			0.115	Mbps
	SP3083, SP3084, SP3085			0.5	
	SP3086, SP3087, SP3088			20	
Operating Free Air Temperature, T_A	Industrial Grade (E)	-40		85	°C

Note: The least positive (most negative) limit is designated as the maxium value.

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Digital Input Signals: DI, DE, $\overline{RE}$							
Logic input thresholds		High, V_{IH}		2.0			V
		Low, V_{IL}				0.8	
Logic Input Current		T_A = 25°C, after first transition				±1	µA
Input Hysteresis		T_A = 25°C			100		mV
Driver							
Differential Driver Output (V_{OD})		No Load				V_{CC}	V
Differential Driver Output, Test 1		R_L=100Ω (RS-422)		2		V_{CC}	V
		R_L=54Ω (RS-485)		1.5	2.7	V_{CC}	
Differential Driver Output, Test 2		V_{CM} = -7 to +12V		1.5		V_{CC}	
Change in Magnitude of Differential Output Voltage (ΔV_{OD}) (Note 1)		R_L=54 or 100Ω				±0.2	V
Driver Common Mode Output Voltage (Vcc)		R_L=54 or 100Ω		1		3	V
Change in Common Mode Output Voltage (ΔV_{OC})		R_L=54 or 100Ω				±0.2	V
Driver Short Circuit Current Limit		-7V ≤ V_{OUT} ≤ +12V				±250	mA
Output Leakage Current (Full-duplex versions, Y & Z pins) Note 2		DE=0,	V_{OUT}=12V			125	µA
		$\overline{RE}$=0, V_{CC}=0 or 5.5V	V_{OUT}= -7V	-100			
Receiver							
Receiver Input Resistance		-7V ≤ V_{CM} ≤ 12V		96			KΩ
Input Current (A, B pins)		DE=0, $\overline{RE}$=0, Vcc=0 or 5.5V	V_{IN}= 12V			125	µA
			V_{IN}= -7V	-100			
Receiver Differential Threshold (VA-VB)		-7V ≤ V_{CM} ≤ 12V		-200	-125	-40	mV
Receiver Input Hysteresis					25		mV
Receiver Output Voltage	V_{OH}	I_{OUT} = -8mA, V_{ID} = -40mV		Vcc-1.5			V
	V_{OL}	I_{OUT} = 8mA, V_{ID} = -200mV				0.4	
High-Z Receiver Output Current		V_{CC} =5.5V, 0 ≤ V_{OUT} ≤ V_{CC}				± 1	µA
Receiver Output Short Circuit Current		0V ≤ V_{RO} ≤ V_{CC}				± 95	mA
Supply and Protection							
Supply Current	IQ, Active Mode	No load, DI=0 or V_{CC}			400	900	µA
	Shutdown Mode	DE=0, $\overline{RE}$=Vcc, DI=V_{CC}				1	µA
Thermal Shutdown Temperature		Junction temperature			165		°C
Thermal Shutdown Hysteresis					15		

Notes:
1. Change in Magnitude of Differential Output Voltage and Change in Magnitude of Common Mode Output Voltage are the changes in output voltage when DI input changes state.
2. Except devices which don't have DE or $\overline{RE}$ inputs.
3. The transceivers are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns the device does not enter shutdown. If the enable inputs are held in this state for at least 600ns the device is assured to be in shutdown. In this low power mode most circuitry is disabled and supply current is typically 1nA.
4.Characterized, not 100% tested.

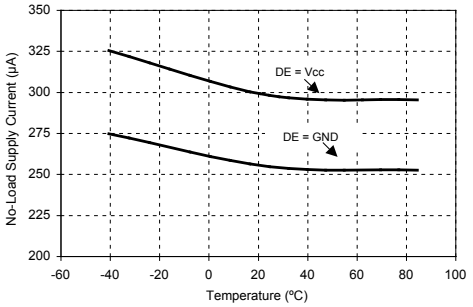
Unless otherwise noted Vcc= +5.0±0.5V, ambient temperature TA from -40 to +85ºC

SP3080E, SP3081E, SP3082E DRIVER CHARACTERISTICS:	Conditions	Min.	Typ.	Max.	Unit
Data Signaling Rate (1 / t_{UI})	Duty Cycle 40 to 60%	115			Kbps
Driver Propagation Delay (t_{PHL}, t_{PLH})	R_L = 54Ω, C_L = 50pF,	500		2600	ns
Driver Output Rise/Fall Time (t_R, t_F)		667	1200	2500	ns
Driver Differential Skew (t_{PLH} – t_{PHL})				±200	ns
Driver Enable to Output High (t_{DZH})	SP3080E, SP3081E			3500	ns
Driver Enable to Output Low (t_{DZL})				3500	ns
Driver Disable from Output High (t_{DHZ})				100	ns
Driver Disable from Output Low (t_{DLZ})				100	ns
Shutdown to Driver Output Valid (t_{DZV})				6000	ns

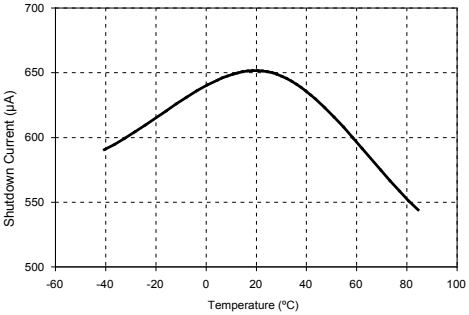
SP3083E, SP3084E, SP3085E DRIVER CHARACTERISTICS:	Conditions	Min.	Typ.	Max.	Unit
Data Signaling Rate (1/ t_{UI})	Duty Cycle 40 to 60%	500			Kbps
Driver Propagation Delay (t_{PHL}, t_{PLH})	R_L = 54Ω, C_L = 50pF,	250		1000	ns
Driver Output Rise/Fall Time (t_R, t_F)		200	530	750	ns
Driver Differential Skew (t_{PLH} – t_{PHL})				±100	ns
Driver Enable to Output High (t_{DZH})	SP3083E, SP3084E			2500	ns
Driver Enable to Output Low (t_{DZL})				2500	ns
Driver Disable from Output High (t_{DHZ})				100	ns
Driver Disable from Output Low (t_{DLZ})				100	ns
Shutdown to Driver Output Valid (t_{DZV})				4500	ns

SP3086E, SP3087E, SP3088E DRIVER CHARACTERISTICS:	Conditions	Min.	Typ.	Max.	Unit
Data Signaling Rate (1 / t_{UI})	Duty Cycle 40 to 60%	20			Mbps
Driver Propagation Delay (t_{PHL}, t_{PLH})	R_L = 54Ω, C_L = 50pF,		12	20	ns
Driver Output Rise/Fall Time (t_R, t_F)			6	10	ns
Driver Differential Skew (t_{PLH} – t_{PHL})				±5	ns
Driver Enable to Output High (t_{DZH})	SP3086E, SP3087E			150	ns
Driver Enable to Output Low (t_{DZL})				150	ns
Driver Disable from Output High (t_{DHZ})				50	ns
Driver Disable from Output Low (t_{DLZ})				50	ns
Shutdown to Driver Output Valid (t_{DZZV})				250	ns

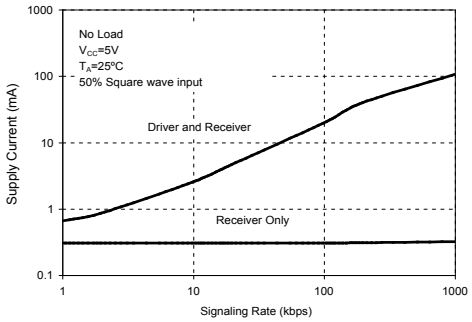
Receiver CHARACTERISTICS:	Conditions	Min.	Typ.	Max.	Unit
Receiver Prop. Delay SP3080E - SP3085E	C_L = 15pF, V_{ID} = ±2V,		75	200	ns
Receiver Prop. Delay SP3086E - SP3088E				75	ns
Prop. Delay Skew SP3080E-SP3085E				±30	ns
Prop. Delay Skew SP3086E-SP3088E				±5	ns
Receiver Output Rise/Fall Time	C_L = 15pf			15	ns
Receiver Enable to Output High (t_{ZH})				50	ns
Receiver Enable to Output Low (t_{ZL})				50	ns
Receiver Disable from High (t_{HZ})				50	ns
Receiver Disable from Low (t_{LZ})				50	ns
Shutdown to Receiver Output Valid (t_{ROV})				3500	ns
Time to Shutdown (Note 2,3,4)		50	200	600	ns



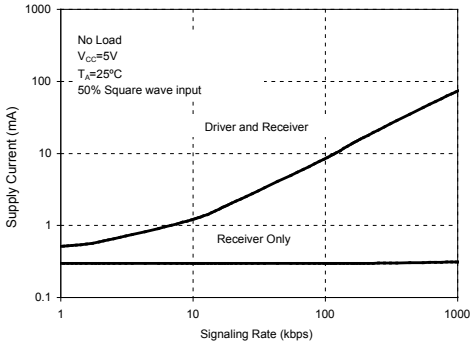
No-load Supply Current vs Temperature



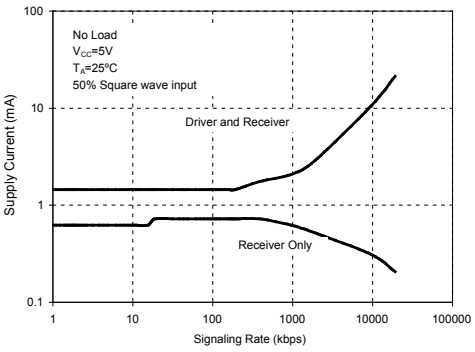
Shutdown Current vs Temperature



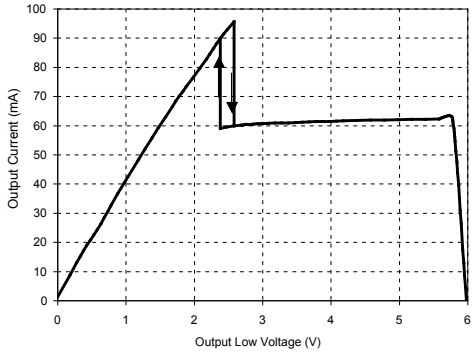
Supply Current vs Signaling Rate (SP3080-SP3082)



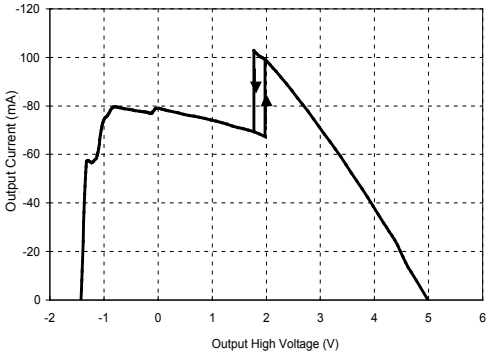
Supply Current vs Signaling Rate (SP3083-SP3085)



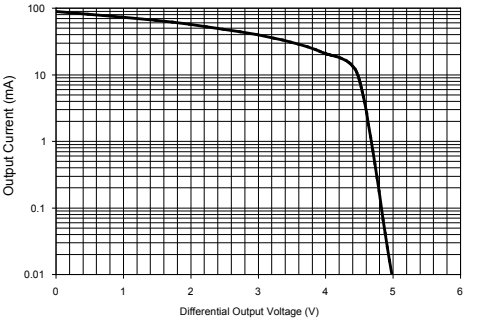
Supply Current vs Signaling Rate (SP3086-SP3088)



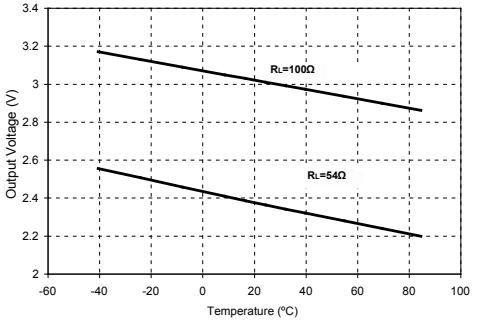
Output Current vs Driver Output Low Voltage



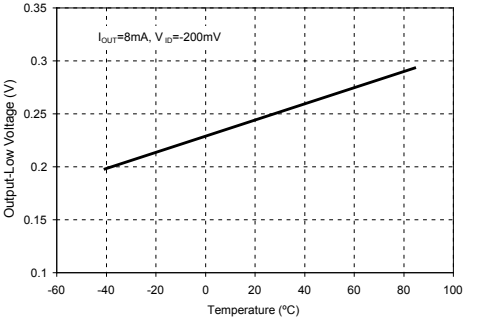
Output Current vs Driver Output High Voltage



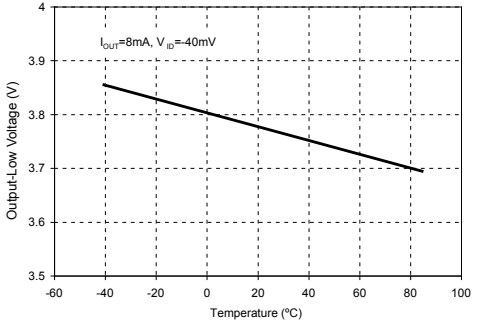
Driver Output Current vs Differential Output Voltage



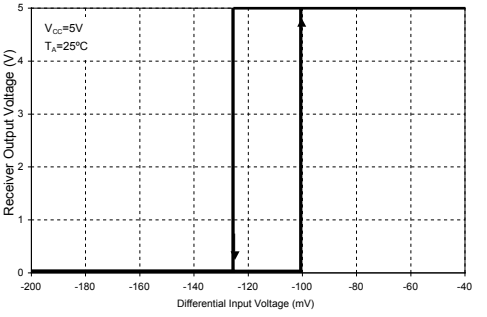
Driver Differential Output Voltage vs Temperature



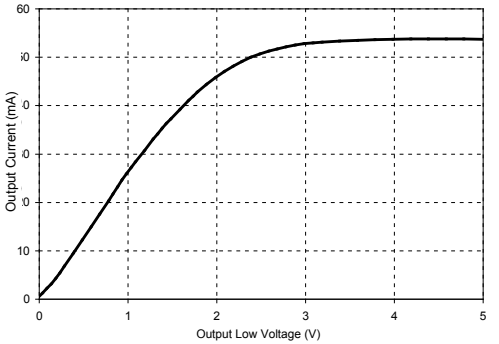
Receiver Output Low Voltage vs Temperature



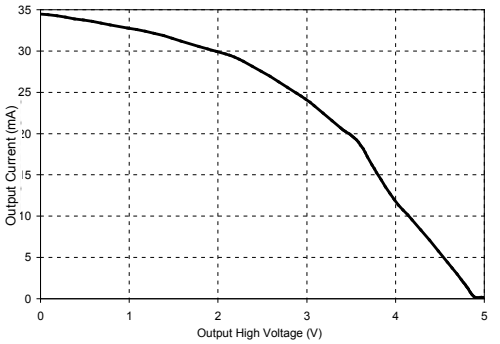
Receiver Output High Voltage vs Temperature



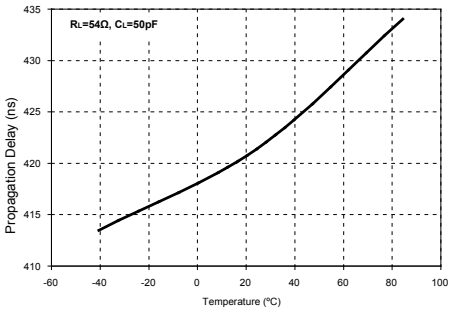
Receiver Output Voltage vs Differential Input Voltage



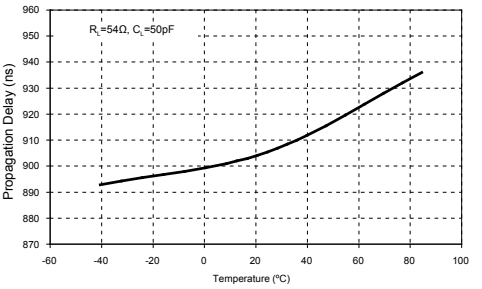
Output Current vs Receiver Low Voltage



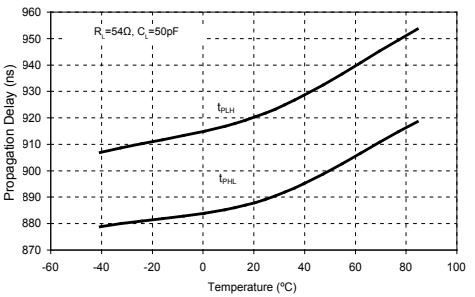
Output Current vs Receiver Output High Voltage



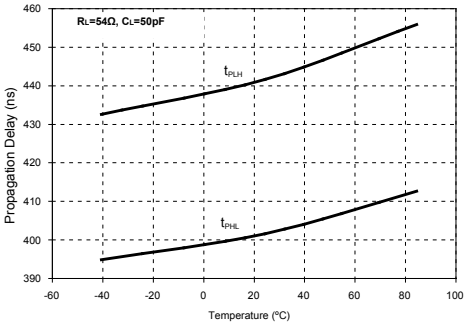
Driver Average Propagation Delay vs Temperature (SP3083-SP3085)



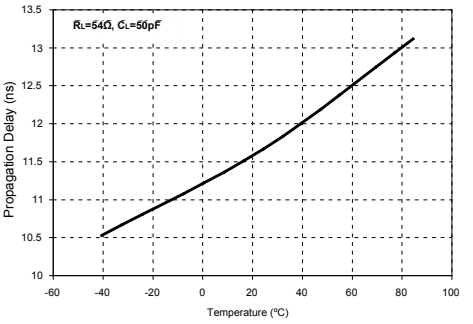
Driver Average Propagation Delay vs Temperature (SP3080-SP3082)



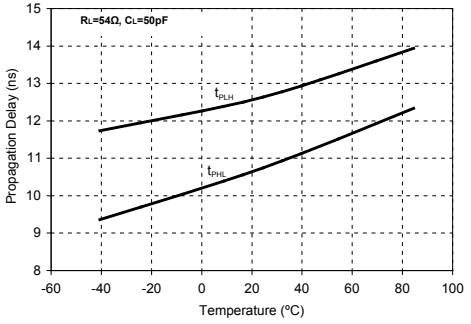
Driver Proagation Delay vs Temerature (SP3080-SP3082)



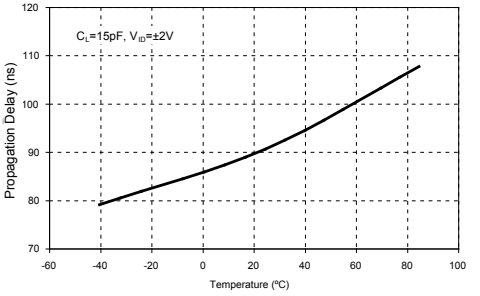
Driver Propagation Delay
vs Temperature (SP3083-SP3085)



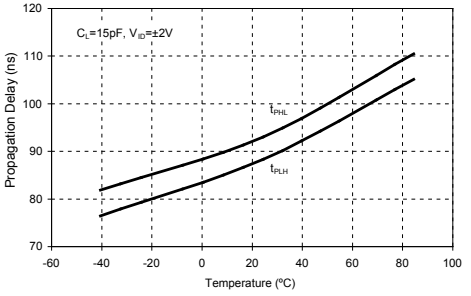
Driver Average Propagation Delay
vs Temperature (SP3086-SP3088)



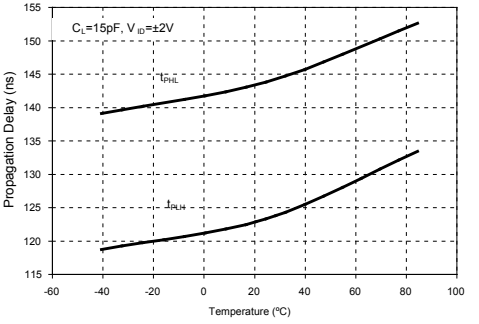
Driver Propagation Delay
vs Temperature (SP3086-SP3088)



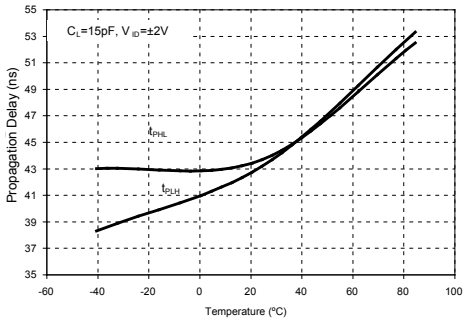
Receiver Average Propagation Delay vs
Temperature (SP3080-SP3082)



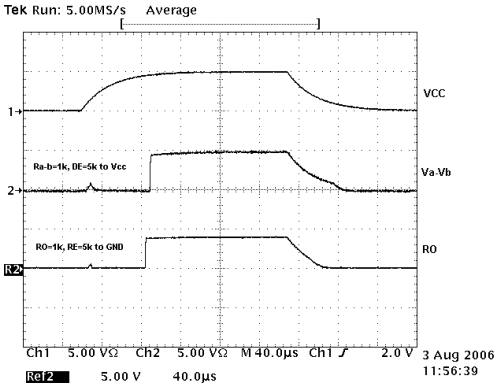
Receiver Propagation Delay vs
Temperature (SP3080-SP3082)



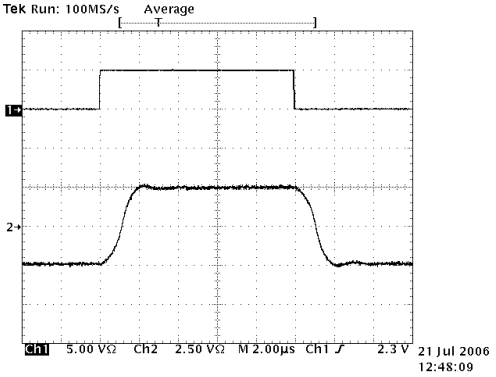
Receiver Propagation Delay
vs Temperature (SP3083-SP3085)



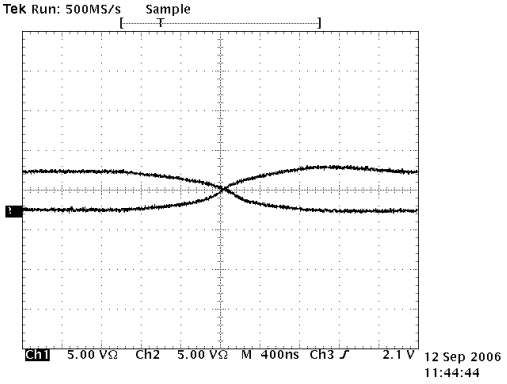
Receiver Propagation Delay
vs Temperature (SP3086-SP3088)



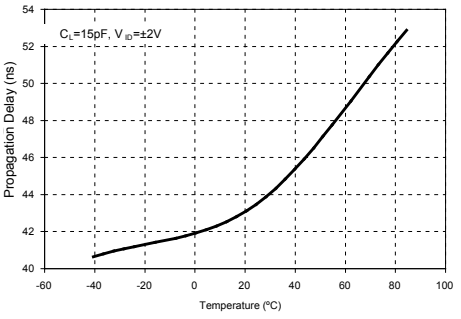
Driver and Receiver Hot Swap
Performance vs. Vcc



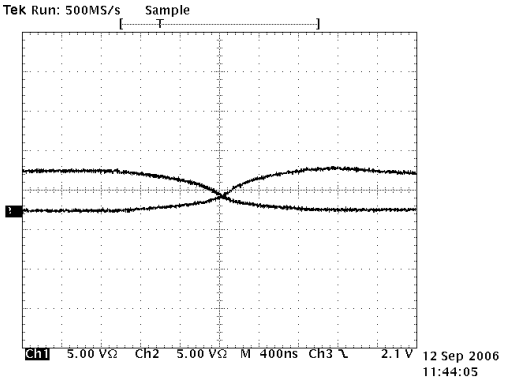
Driver Propagation Delay
(SP3080-SP3082)



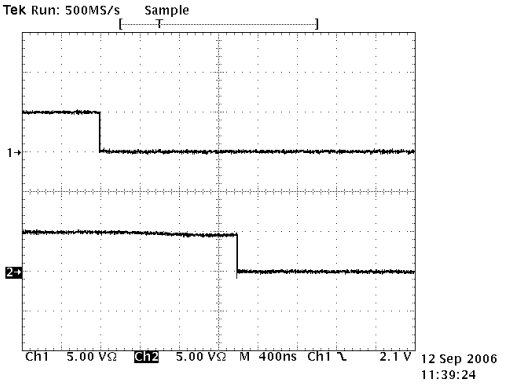
Driver output Waveform
Low to High (SP3080-SP3082)



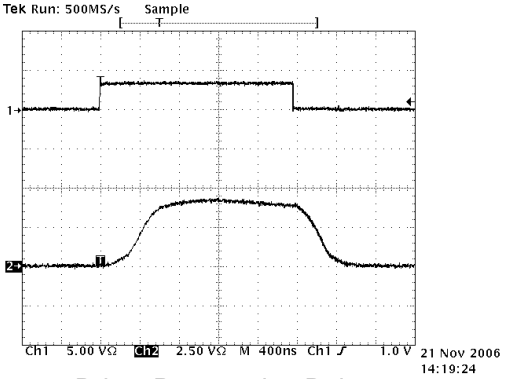
Receiver Average Propagation Delay vs
Temperature (SP3086-SP3088)



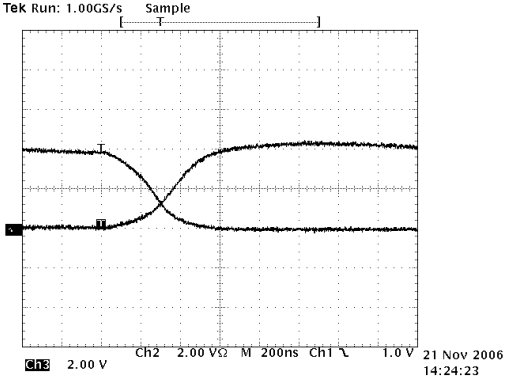
Driver output Waveform
High to Low (SP3080-SP3082)



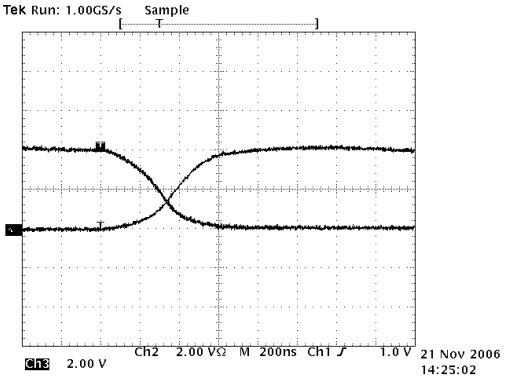
Driver and Receiver Waveform
High to Low (SP3080-SP3082)



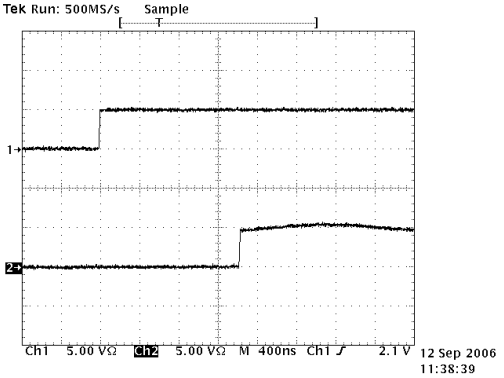
Driver Propagation Delay
(SP3083-SP3085)



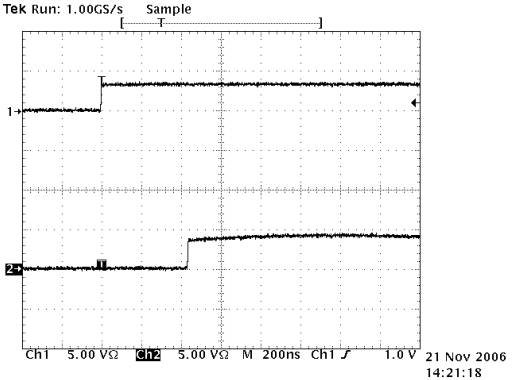
Driver Output Waveform
Low to High (SP3083-SP3085)



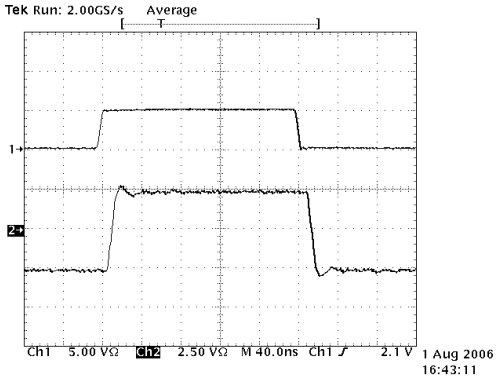
Driver Output Waveform
High to Low (SP3083-SP3085)



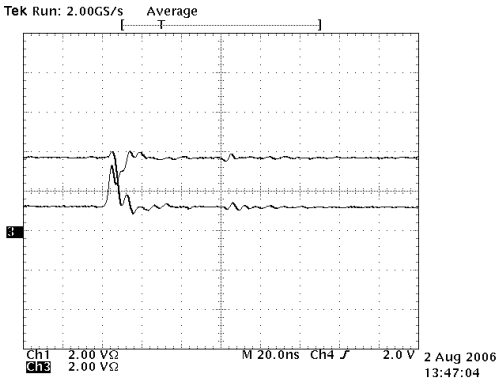
Driver and Receiver Waveform
Low to High (SP3080-SP3082)



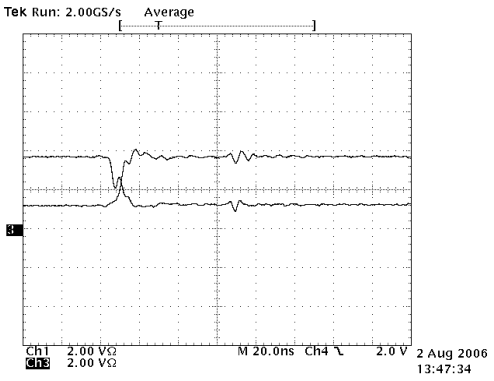
Driver and Receiver Waveform
Low to High (SP3083-SP3085)



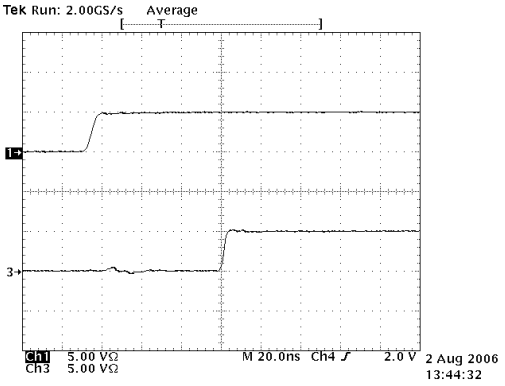
Driver Propagation Delay
(SP3086-SP3088)



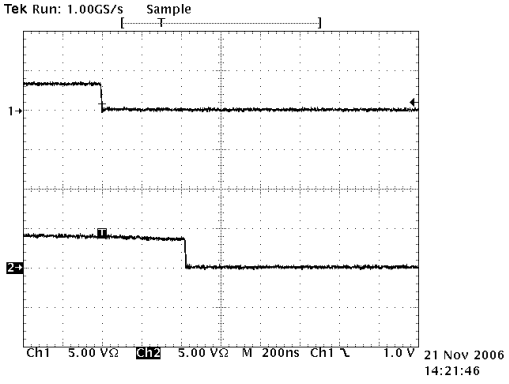
Driver Output Waveform
Low to High (SP3086-SP3088)



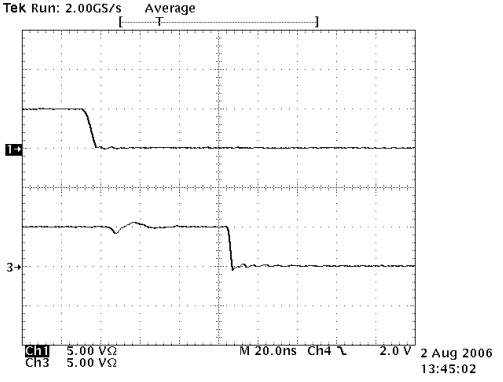
Driver Output Waveforms
High to Low (SP3086-SP3088)



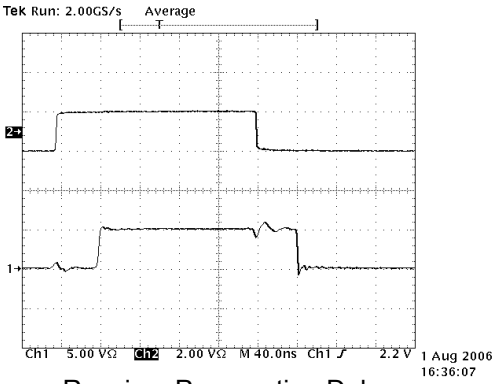
Driver and Receiver Waveform
Low to High (SP3086-SP3088)



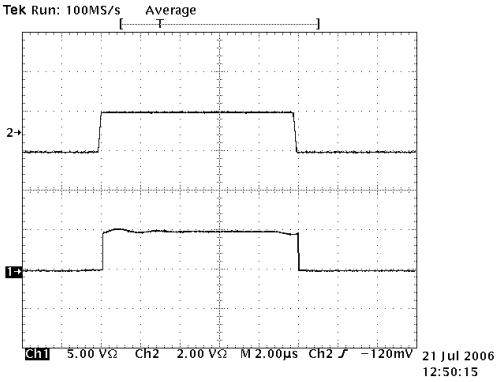
Driver and Receiver Waveform
High to Low (SP3083-SP3085)



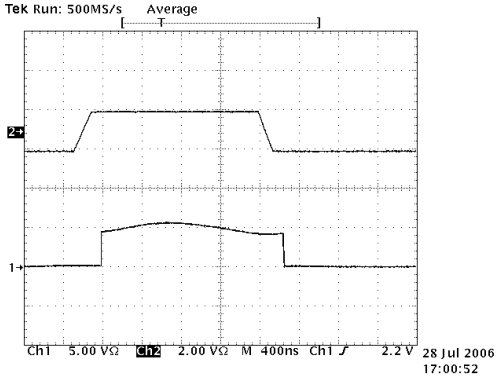
Driver and Receiver Waveform
High to Low (SP3086-SP3088)



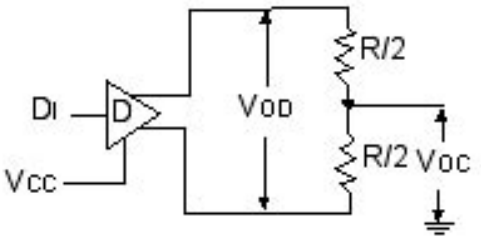
Receiver Propagation Delay
(SP3086-SP3088)



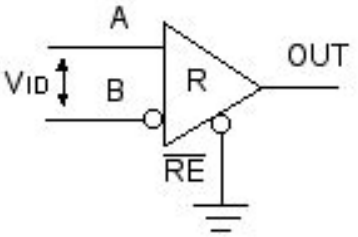
Receiver Propagation Delay
(SP3080-SP3082)



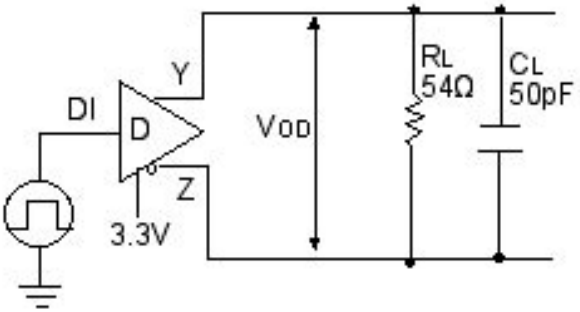
Receiver Propagation Delay
(SP3083-SP3085)



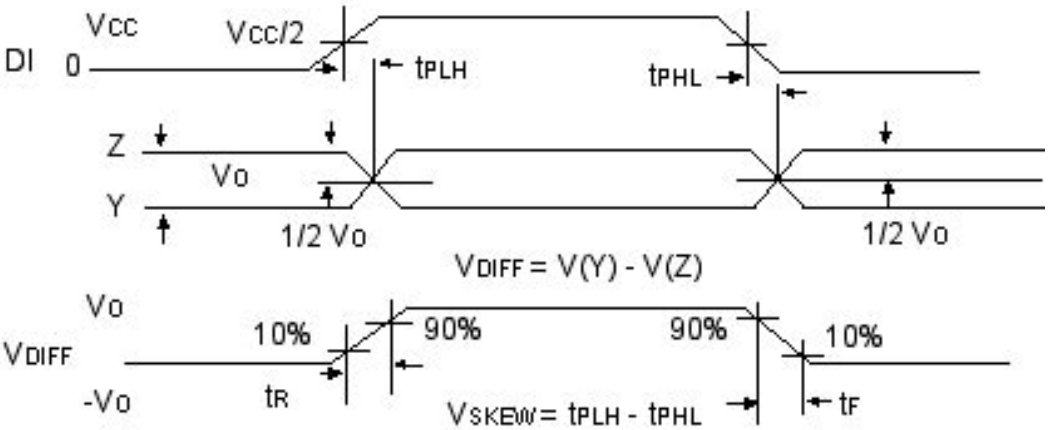
Driver DC Test Circuit



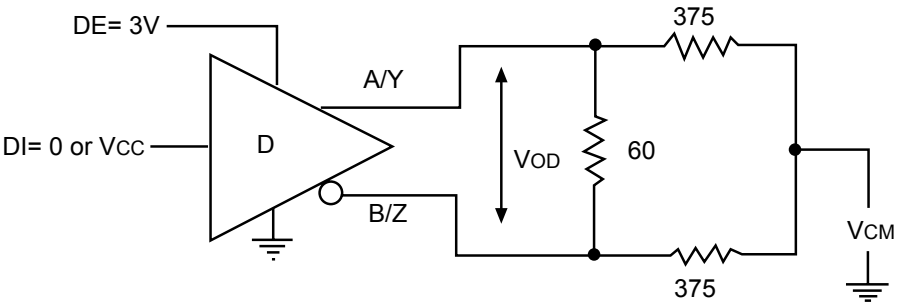
Receiver DC Test Circuit



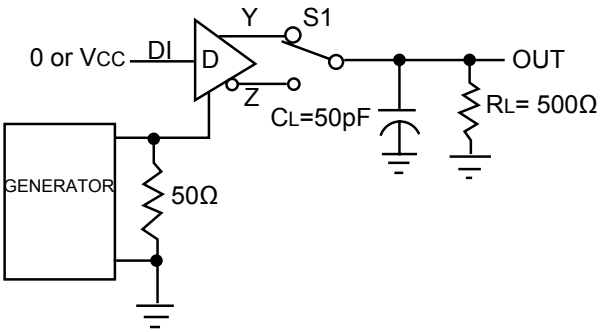
Driver Propagation Delay Time Test Circuit and Timing Diagram

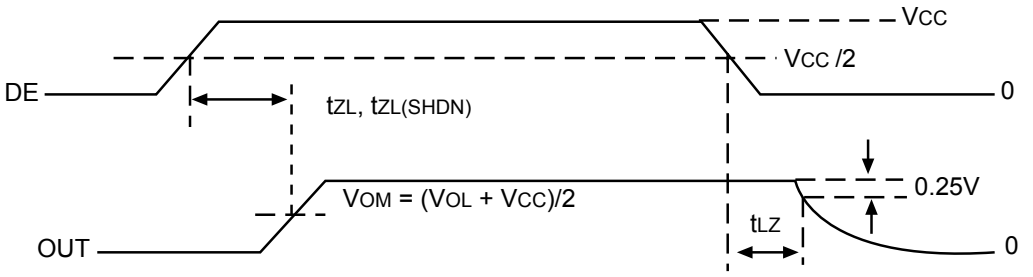


Driver Differential Output Test Circuit

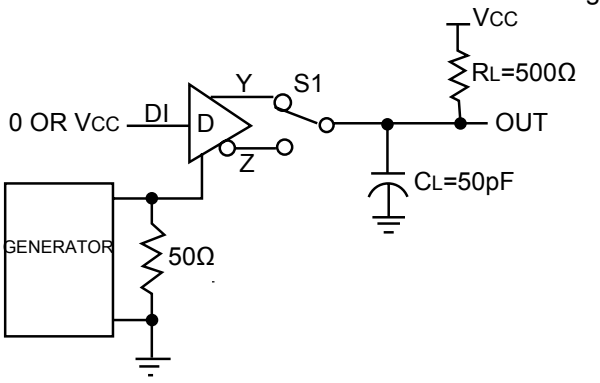


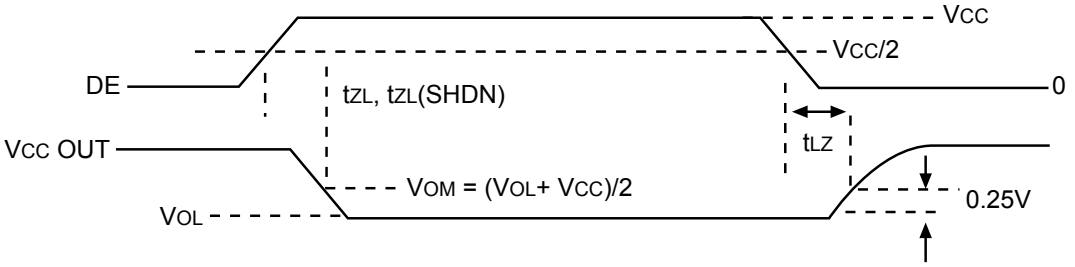
Driver Enable and Disable Times Test Circuit and Timing Diagram



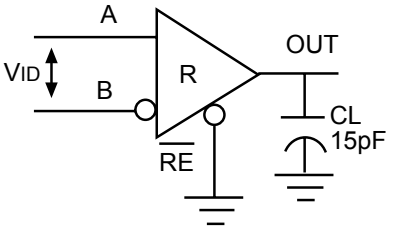


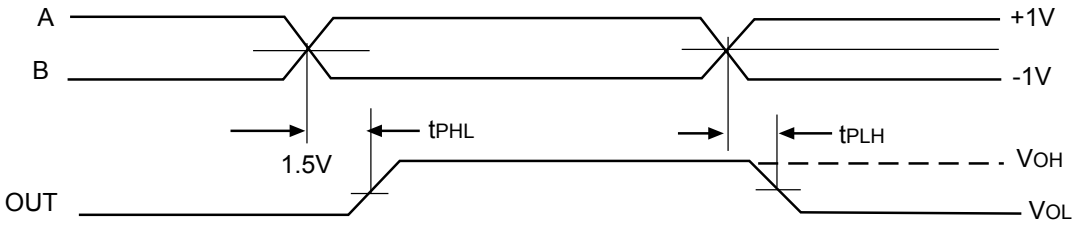
Driver Enable and Disable Times Test Circuit and Timing Diagram



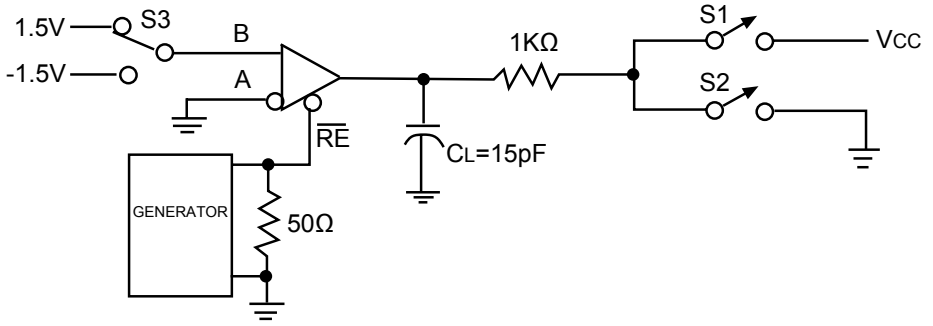


Receiver Propagation Delay Test Circuit and Timing Diagram



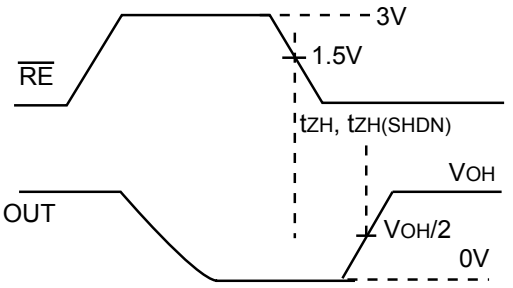


Receiver Enable and Disable Times Test Circuit

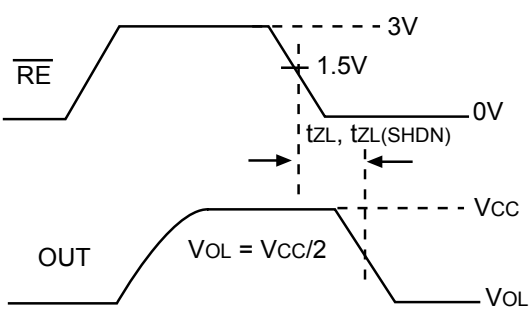


Receiver Enable and DisableTiming Diagram

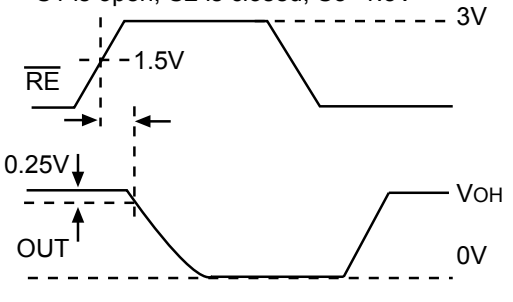
S1 is open, S2 is closed, S3=1.5V



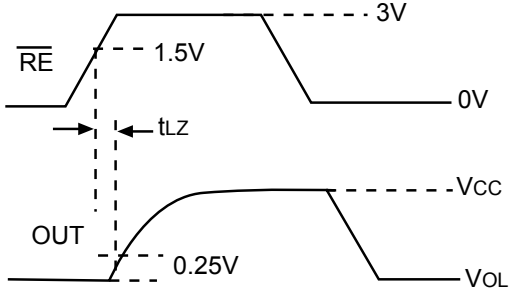
S1 is closed, S2 is open, S3= -1.5V



S1 is open, S2 is closed, S3=1.5V



S1 is closed, S2 is open, S3= -1.5V



FUNCTION TABLES

SP3080E, SP3083E, SP3086E (Full Duplex)

Transmitting				
Inputs			Outputs	
$\overline{RE}$	DE	DI	Y	Z
X	1	1	1	0
X	1	0	0	1
0	0	X	High-Z	
1	0	X	Shutdown	

Receiving			
Inputs			Output
$\overline{RE}$	DE	$V_A - V_B$	RO
0	X	≥ -40mV	1
0	X	≤-200mV	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	Shutdown

SP3081E SP3084E, SP3087E (Full Duplex)

Transmitting		
Input	Outputs	
DI	Y	Z
1	1	0
0	0	1
Open	1	0

Receiving	
Inputs	Output
$V_A - V_B$	RO
≥ -40mV	1
≤-200mV	0
Open/shorted	1

SP3082E SP3085E, SP3088E (Half Duplex)

Transmitting				
Inputs			Outputs	
$\overline{RE}$	DE	DI	A	B
X	1	1	1	0
X	1	0	0	1
0	0	X	High-Z	
1	0	X	Shutdown	

Receiving			
Inputs			Output
$\overline{RE}$	DE	$V_A - V_B$	RO
0	X	≥ -40mV	1
0	X	≤-200mV	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	Shutdown

Note: Receiver inputs -200mV < VA - VB < -40mV, should be considered indeterminate

PRODUCT SELECTOR GUIDE

Part Number	Duplex	Data Rate (Mbps)	Shut-down	Receiver & Driver Enable	Trans on Bus	Foot-print	pin-compatible upgrade from:
SP3080E	Full	0.115	Yes	Yes	256	SN75180	MAX3080
SP3081E	Full	0.115	No	No	256	SN75179	MAX3081
SP3082E	Half	0.115	Yes	Yes	256	SN75176	SP483, MAX3082
SP3083E	Full	0.5	Yes	Yes	256	SN75180	MAX3083
SP3084E	Full	0.5	No	No	256	SN75179	MAX3084
SP3085E	Half	0.5	Yes	Yes	256	SN75176	MAX3085
SP3086E	Full	20	Yes	Yes	256	SN75180	SP1491, MAX3086
SP3087E	Full	20	No	No	256	SN75179	SP1490, MAX3087
SP3088E	Half	20	Yes	Yes	256	SN75176	SP1481, MAX3088

DETAILED DESCRIPTION

SP3080E-SP3088E is a family of advanced RS-485/RS-422 transceivers. Each contains one driver and one receiver. These devices feature fail-safe circuitry that guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled. SP3080E, SP3082E, SP3083E, SP3085E, SP3086E and SP3088E also feature a hot-swap capability allowing live insertion without error data transfer.

The SP3080E, SP3081E and SP3082E feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 115kbps. The SP3083E, SP3084E and SP3085E also offer slew-rate limits allowing transmit speeds up to 500kbps. The SP3086E, SP3087E, SP3088E driver slew rates are not limited, making transmit speeds up to 20Mbps possible.

The SP3082E, SP3085E and SP3088E are half-duplex transceivers, while the SP3080E, SP3081E, SP3083E, SP3084E, SP3086E, and SP3087E are full duplex transceivers.

All devices operate from a single 5.0V supply. Drivers are output short-circuit current limited. Thermal-shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal-shutdown circuitry places the driver outputs into a high-impedance state.

RECEIVER INPUT FILTERING

SP3080E-SP3085E receivers incorporate input filtering in addition to input hysteresis. This filtering enhances noise immunity with differential signals that have very slow rise and fall times. Receiver propagation delay increases due to this filtering.

ADVANCED FAIL SAFE

Ordinary RS485 differential receivers will be in an indeterminate state whenever A - B is less than ±200mV. This situation can occur whenever the data bus is not being actively driven. The Advanced Failsafe feature of the SP3080E family guarantees a logic-high receiver output if the receiver's differential inputs are shorted, open-circuit, or if they are shunted by a termination resistor.

The receiver thresholds of the SP3080E family, are very precise and offset by at least a 40mV noise margin from ground. This results in a logic-high receiver output at zero volts input differential while maintaining compliance with the EIA/TIA-485 standard of ±200mV.

HOT-SWAP CAPABILITY

When a micro-processor or other logic device undergoes its power-up sequence its logic-outputs are typically at high impedance. In this state they are unable to drive the DE and signals to a defined logic level. During this period, noise, parasitic coupling or leakage from other devices could cause standard CMOS enable inputs to drift to an incorrect logic level.

If circuit boards are inserted into an energized backplane (commonly called "live insertion" or "hot-swap") power may be suddenly applied to all circuits. Without the hot-swap capability, this situation could improperly enable the transceiver's driver or receiver, driving invalid data onto shared busses and possibly causing driver contention or device damage.

The SP3080E family contains a special power-on-reset circuit that holds DE low and $\overline{RE}$ high for approximately 10 microseconds. After this initial power-up sequence the hot-swap circuit becomes transparent, allowing for normal, unskewed enable and disable timings.

±15KV ESD PROTECTION

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver output and receiver inputs of the SP3080E family have extra protection against static electricity. Sipex uses state of the art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the SP3080E - SP3088E keeps working without latch-up or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of

the SP3080E - SP3088E are characterized for protection to the following limits:

±15kV using the Human Body Model
±8kV using the Contact Discharge method specified in IEC 1000-4-2
±15kV Air-gap

ESD TEST CONDITIONS

ESD performance depends on a variety of conditions. Contact Sipex for a reliability report that documents test setup, methodology and results.

IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The SP3080E family helps you design equipment to meet IEC 1000-4-2, without sacrificing board space and cost for external ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 1000-4-2 is a higher peak current in IEC 1000-4-2 series resistance is lower in the IEC 1000-4-2 model. Hence, the ESD withstand voltage measured to IEC 1000-4-2 is generally lower than that measured using the human body model.
The air-gap test involves approaching the device with a charged probe. The contact discharge method connects the probe to the device before the probe is energized.

MACHINE MODEL

The machine model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. The objective is to emulate the stress caused when I/O pins are contacted by handling equipment during test and assembly.

256 TRANSCEIVERS ON THE BUS

The standard RS-485 receiver input impedance is 12kΩ (1 unit load). A standard driver can drive up to 32 unit loads. The SP3080E family of transceivers has only a 1/8th unit load receiver input impedance (96kΩ), thereby allowing eight times as many, up to 256, transceivers to be connected in parallel on a communication line. Any combination of these devices and other RS-485 transceivers up to a total of 32 unit loads may be connected to the line.

LOW POWER SHUTDOWN MODE

Low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low simultaneously. While in shutdown devices typically draw only 50nA of supply current. DE and $\overline{RE}$ may be tied together and driven by a single control signal. Devices are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are shutdown.

Enable times t_{ZH} and t_{ZL} apply when the part is not in low-power shutdown state. Enable times $t_{ZH}(\overline{SHDN})$ and $t_{ZL}(\overline{SHDN})$ apply when the parts are shut down. The drivers and receivers take longer to become enabled from low power shutdown mode $t_{ZL}(\overline{SHDN})$ and $t_{ZL}(\overline{SHDN})$ than from driver/receiver-disable mode (t_{ZH}, t_{ZL}).

DRIVER OUTPUT PROTECTION

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. First, a driver-current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range. Second, a thermal-shutdown circuit forces the driver outputs into a high-impedance state if junction temperature becomes excessive.

LINE LENGTH, EMI, AND REFLECTIONS

SP3080E - SP3085E feature controlled slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables.

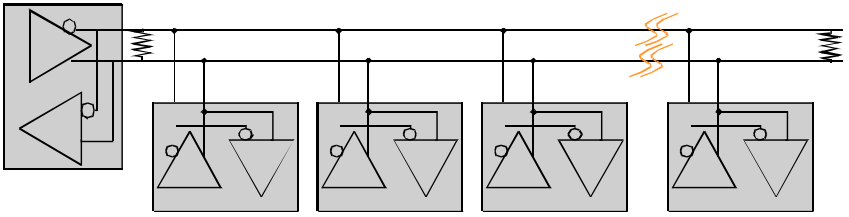
SP3080E - SP3083E driver rise and fall times are limited to no faster than 667ns, allowing error-free data transmission up to 115kbps. The SP3083, SP3084 and SP3085 offer somewhat higher driver output slew-rate limits, allowing transmit speeds up to 500kbps.

The RS-485/RS-422 standard covers line lengths up to 4,000ft. Maximum achievable line length is a function of signal attenuation and noise. Use of slew-controlled drivers such as the SP3080E-SP3086E may help to reduce crosstalk interference and permit communication over longer transmission lines.

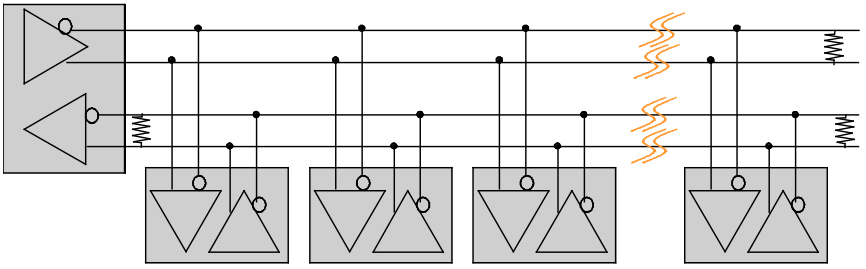
Termination prevents reflections by eliminating the impedance mismatches on a transmission line. Line termination is typically used if rise and fall times are shorter than the round-trip signal propagation time. Slew-limited drivers may reduce or eliminate the need for cable termination in many applications.

TYPICAL APPLICATIONS:

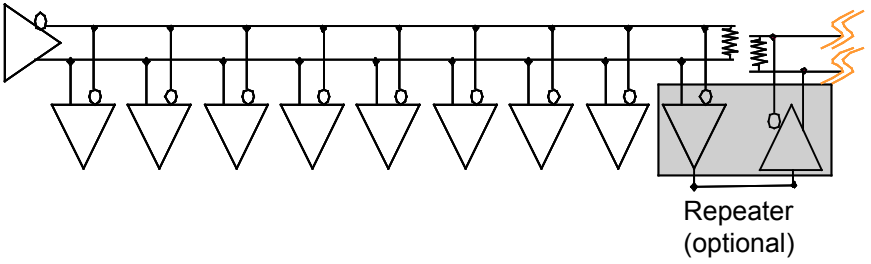
Half-Duplex Network



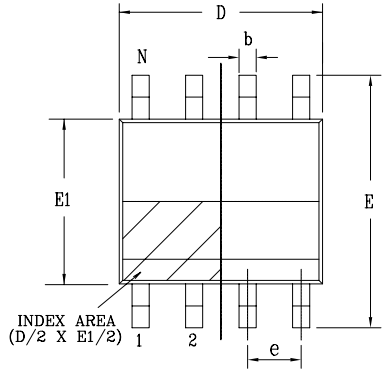
Bi-Directional Full-Duplex Network



Point to Multi-Point Repeater

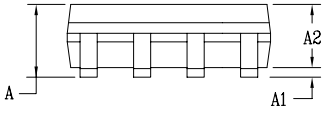


REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/16/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL

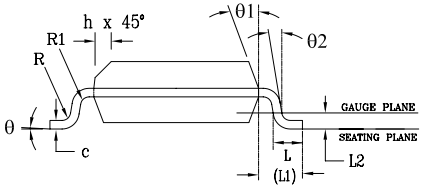


Top View

8 Pin SOICN JEDEC MS-012 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	4.90 BSC			0.193 BSC		
N	8			8		



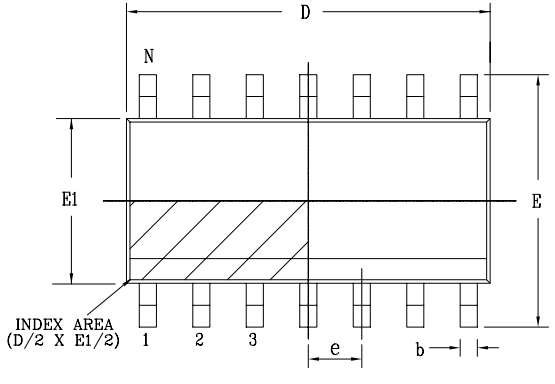
Side View



Front View

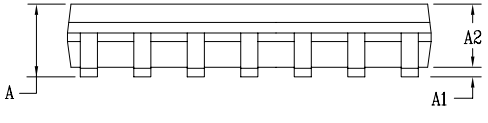
Sipex	SIPEX CORPORATION		
	8 PIN SOICN PACKAGE OUTLINE		
Packaging Approval:	Drawing No: 8-PIN SOICN		
By: JL / Date: 07/19/06	Revision: B	Sheet: 1 OF 1	

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	04/17/06	JL

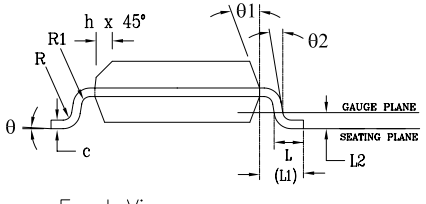


Top View

14 Pin SOICN JEDEC MS-012 Variation AB						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	8.65 BSC			0.341 BSC		
N	14			14		



Side View



Front View

Sipex	SIPEX CORPORATION		
	14 PIN SOICN PACKAGE OUTLINE		
Packaging Approval:	Drawing No: 14-PIN SOICN		
By: JL / Date: 04/17/06	Revision: A	Sheet: 1 OF 1	

Part number	LEAD FREE	Tape & Reel	Temperature range	Package Type
SP3080EEN	**-L**	**/TR**	From -40 to +85^{0}C	14 pin nSOIC
SP3081EEN	**-L**	**/TR**	From -40 to +85^{0}C	8 pin nSOIC
SP3082EEN	**-L**	**/TR**	From -40 to +85^{0}C	8 pin nSOIC
SP3083EEN	**-L**	**/TR**	From -40 to +85^{0}C	14 pin nSOIC
SP3084EEN	**-L**	**/TR**	From -40 to +85^{0}C	8 pin nSOIC
SP3085EEN	**-L**	**/TR**	From -40 to +85^{0}C	8 pin nSOIC
SP3086EEN	**-L**	**/TR**	From -40 to +85^{0}C	14 pin nSOIC
SP3087EEN	**-L**	**/TR**	From -40 to +85^{0}C	8 pin nSOIC
SP3088EEN	**-L**	**/TR**	From -40 to +85^{0}C	8 pin nSOIC

All packages are available as lead free (RoHS compliant). To order add “-L” suffix to part number. For Tape and Reel add “/TR”. Reel quantity is 2,500 for NSOIC.

Example: SP3082EEN-L/TR = lead free and Tape and Reel. SP3082EEN/TR = standard with Tape and Reel.

Solved by Sipex™

Sipex Corporation

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5/18/06	A	Created datasheet from PDS	G. DIXON
6/1/2006	B	Visual Standards changes	
6/11/06	C	Visual Standards Changes	S. Pena
11/27/06	D	Formatting changes.	H. Wong
11/30/06	E	Inserted high speed curves	H. Wong
12/5/06	F	Labeld high speed curves,margins, spelling	H. Wong/ Design
12/6/06	G	Reordered curves, font sizes in notes, new package drawings	H. Wong
12/6/06	H	Notes on page 4.	H. Wong
12/8/06	I	Page1: slew rate, shorted page2: swap 8 pin full dulpex for 8 pin 1/2 duplex pg8: replaced Receiver Vout vs Diff Vin curve pg10: deleted receiver average prop delay curve, fixed typo pg17: fixed typo	H.Wong/ Design/ Apps/ Marketing
12/8/06	J	Removed references to extended temp range	H. Wong
12/12/06	K	Pg4: removed Junction temp line	H. Wong
12/21/07	L	Deleted Driver Diff. Skew vs. Temp grpah on page 9. Could not export document at once	H. Wong
12/22/07	M	Used mac to export document.	

This information is not to be given out to customers

